CLOCK DATA RECOVERY CIRCUITRY AND
PHASE LOCKED LOOP CIRCUITRY WITH
DYNAMICALLY ADJUSTABLE BANDWIDTHS

[0064] Clock data recovery (CDR) circuitry or phase locked loop (PLL) circuitry can be provided with a dynamically adjustable bandwidth. One CDR circuit or PLL circuit can be provided to support multiple systems or protocols, multiple parameter requirements for a given system or protocol, and changes in the input frequency or data rate within a given system or protocol. The parameters can include jitter (e.g., jitter tolerance, jitter transfer, jitter generation), source of dominant noise, and lock time. Control signals can be used to dynamically adjust the bandwidth of the CDR circuitry or PLL circuitry while the circuitry is processing data. The control signals can be set by a PLD, by a processor, by circuitry external to the PLD, or by user input.